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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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VOLPE AND KOENIG, P.C.
DEPT. ICC
UNITED PLAZA, SUITE 1600
30 SOUTH 17TH STREET
PHILADELPHIA, PA 19103

EXAMINER	
WANG, TED M	
ART UNIT	**PAPER NUMBER**
2634	

DATE MAILED: 05/25/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/629,429	DEMIR, ALPASLAN	
	Examiner	Art Unit	
	Ted M. Wang	2634	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 February 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *5-8,17 and 18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *5-8,17 and 18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *7/29/2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *3/28/2005*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. The indicated allowability of claims 5-8, 17, and 18 are withdrawn in view of the newly discovered reference(s) to US 5,994,932. Rejections based on the newly cited reference(s) follow.

Information Disclosure Statement

2. The document numbers US 6,236,343, US 6,775,318, US 6,804,315, and US 2001/0021199 listed in the information disclosure statement filed on March 28 2005 have not been considered because they have been cited by the examiner previously in the office action, PTO-892, paper number 12062004.

Claim Objections

3. Claims 17 and 18 are objected to because of the following informalities:

- In claims 17 and 18, line 1, change 'method" to --- system ---.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 5-8 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lee et al. (US 2001/0021199) in view of Ando (US 5,994,932).

- With regard claim 5, Lee et al. discloses a system comprises:

  a first correlator (Fig.5 element 500) for receiving a first stored sequence of the primary synchronization channel (paragraphs 35 and 36);

  a second correlator (Fig.5 element 501) for receiving a second stored sequence of the primary synchronization channel (paragraphs 35 and 36);

  an error estimator (Fig.3 element 261 and Fig.5) for determining the error associated with the outputs of the first and second correlators (Fig.3 element 302 output ω and Fig.5 element 550 output ω); and

  a voltage controlled oscillator (NCO) for adjusting frequency responsive to the integrated error estimate (Fig.3 element 303).

  Lee et al. discloses all of the subject matter as described in the above paragraph except for specifically teaching a filter for selectively integrating the error estimate responsive to an initial or steady state conditions of the cell search process;

  However, Ando teaches that a filter for selectively integrating the error estimate responsive to an initial or steady state conditions (Fig.1 element 103 and column 1 lines 30-40).

  It is desirable to have a filter for selectively integrating the error estimate responsive to an initial or steady state conditions in order to smooth the DC control voltage.

  Therefore, It would have been obvious to one of ordinary skill in the art at the time of the invention was made to include the PLL circuit as taught by Ando in which, a

filter for selectively integrating the error estimate responsive to an initial or steady state conditions, into Lees' PLL circuit so as to smooth the DC control voltage.

- With regard claim 6, Lee et al. further discloses that the given sequence is a primary synchronization code (PSC) sequence (paragraphs 35 and 36).
- With regard claim 17, Lee et al. further discloses that the frequency adjustment is numerically controlled (Fig.3 element 303).
- With regard to claim 18, Lee et al. discloses all of the subject matter as described in the above paragraph except for specifically teaching that the frequency adjustment is voltage controlled (VCO) instead of numerically controlled (NCO).

  However, Ando teaches that the frequency adjustment is voltage controlled (VCO) (Fig.1 element 103 and column 1 lines 30-40), which is an equivalent structure known in the art. Therefore, because these two (VCO is designed for an analog PLL circuit and NCO is designed for a digital PLL circuit) were art-recognized equivalents at the time the invention was made, one of ordinary skill in the art would have found it obvious to substitute the frequency adjustment VCO to the frequency adjustment NCO.

6. Claims 7 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lee et al. (US 2001/0021199) and Ando (US 5,994,932) as applied to claim 5 above, and further in view of Patapoutian (US 6,236,343).

- With regard claim 7, Lee et al. and Ando disclose all of the subject matter as described in the above paragraph except for specifically teaching that the filter is a proportional integral (PI) filter.

However, Patapoutian teaches that the filter is a proportional integral (PI) filter (Fig.1 element 29 and column 1 lines 45-62).

It is desirable that the filter is a proportional integral (PI) filter in order to minimize the jitter of the PLL circuit and reduce the sensitivity to large bursty noises (column 2 lines 15-29). Therefore, It would have been obvious to one of ordinary skill in the art at the time of the invention was made to include the PI loop filter as taught by Patapoutian into Lee et al. and Andos' PLL circuit so as to minimize the jitter of the PLL circuit and reduce the sensitivity to large bursty noises.

- With regard claim 8, Lee et al. and Ando disclose all of the subject matter as described in the above paragraph except for specifically teaching that the filter having a delay element of $1/(1-z^{-1})$.

  However, Patapoutian (cited previously) teaches that the filter is a proportional integral (PI) filter having a delay element of $1/(1-z^{-1})$ (Fig.1 element 18 and column 1 lines 46-60).

  It is desirable that the filter is a proportional integral (PI) filter having a delay element of $1/(1-z^{-1})$ in order to minimize the jitter of the PLL circuit and reduce the sensitivity to large bursty noises (column 2 lines 15-29). Therefore, It would have been obvious to one of ordinary skill in the art at the time of the invention was made to include the PI loop filter a delay element of $1/(1-z^{-1})$ as taught by Patapoutian into Lee et al. and Andos' PLL circuit so as to minimize the jitter of the PLL circuit and reduce the sensitivity to large bursty noises.

Conclusion

7. Reference(s) US 6,597,729 and GB 2377126A are cited because they are put pertinent to the carrier frequency estimation of initial frequency acquisition for WCDMA mobile terminal. However, none of references teach detailed connection as recited in claim.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ted M. Wang whose telephone number is 571-272-3053. The examiner can normally be reached on M-F, 7:30 AM to 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Stephen Chin can be reached on 571-272-3056. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Ted M Wang
Examiner
Art Unit 2634

Ted M. Wang

SHUWANG LIU
PRIMARY EXAMINER